Amendments to the Claims:

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method for a network switch, the method comprising:

counting statistics for a plurality of connections, wherein the statistics include a number of cells per virtual channel and a number of cells having a loss priority bit;

determining if a count value for each of the connections is above a threshold; and

collecting statistics for the connections of the switch having the count value above the threshold before connections having the count value below the threshold.

2. (Previously Presented) The method of claim 1, wherein the threshold is a percentage of a maximum count limit, wherein the percentage is calculated to ensure the statistics are collected before the maximum count limit is reached.

3. (Currently Amended) The method of claim 1, wherein determining if the count value for each of the connections is above the threshold includes:

sending an interrupt signal from a counter to a processor for each connection having a determined count value above the threshold indicating that the statistics have a high priority.

4. (Currently Amended) The method of claim 3, wherein collecting statistics for the connections

includes:

collecting statistics for connections with ~~corresponding~~ interrupt signals before other connections without ~~with no corresponding~~ interrupt signals.

5. (Previously Presented) The method of claim 3, wherein sending an interrupt signal includes:

placing a logical connection identifier for each statistic having an associated count value above the threshold, wherein the logical connection identifier is placed in a first-in-first-out (FIFO) buffer.

6. (Original) The method of claim 5, wherein collecting statistics for connections includes:

reading statistics in a memory based on the logical connection identifiers stored in the FIFO buffer.

7. (Currently Amended) An apparatus comprising:

one or more counters, each counter to count statistics for a connection, wherein the statistics include a number of cells per connection and a number of cells having a loss priority bit; and

a processor to determine if a count value for each of the counters is above a threshold and to collect the statistics for the connections of a ~~the~~ switch from counters having ~~a~~ the count value above the threshold before counters having ~~a~~ the count value below the threshold.

8. (Cancelled)

9. (Currently Amended) The apparatus of claim 7, wherein each counter is to send an interrupt signal from the one or more counters to a processor for each ~~a respective~~ connection having the ~~a determined~~ count value above the threshold indicating that the statistics have a high priority.

10. (Currently Amended) The apparatus of claim 9, wherein the processor is to collect statistics from ~~for~~ counters ~~having corresponding~~ sending interrupt signals before other counters without ~~with no corresponding~~ interrupt signals.

11. (Original) The apparatus of claim 9, further comprising:

a first-in-first-out (FIFO) buffer to store logical connection identifiers, each logical connection identifier to be used to collect high priority statistics.

12. (Original) The apparatus of claim 11, further comprising:

a memory to store statistics, wherein the processor is to read high priority statistics in the memory based on the logical connection identifiers stored in the FIFO buffer.

13. (Currently Amended) A network interface comprising:

a memory to store statistics for a connection, wherein the statistics include a number of cells per connection and a number of cells having a loss priority bit;

one or more counters, each counter to count statistics stored in the memory;

a processor to determine if a count value for each of the counters is above a threshold and to collect the statistics for the connections of a ~~the~~ switch stored in the memory derived from counters having ~~a~~ the count value above the threshold before collecting statistics in the memory derived from counters having ~~a~~ the count value below the threshold.

14. (Cancelled)

15. (Currently Amended) The network interface of claim 13, wherein each counter is to send an interrupt signal from the one or more counters to the processor for each ~~a respective~~

connection having the ~~a determined~~ count value above the threshold indicating that the statistics have a high priority.

16. (Currently Amended) The network interface claim 15, wherein the processor is to collect statistics ~~for~~ from counters having ~~with corresponding~~ sent interrupt signals before other counters without ~~with no~~ interrupt signals.

17. (Original) The network interface of claim 15, further comprising:

a first-in-first-out (FIFO) buffer to store logical connection identifiers, each logical connection identifier to be used to collect high priority statistics.

18. (Original) The network interface of claim 17, further comprising:

a memory to store statistics, wherein the processor is to read high priority statistics in the memory based on the logical connection identifiers in the FIFO buffer.

19. (Original) The network interface of claim 13, further comprising:

one or more ports, each port receiving or forwarding traffic cells.

20. (Original) The network interface of claim 19, wherein the one or more ports are optical carrier (OC) ports, synchronous transport system (STS) ports, or synchronous digital hierarchy (SDH) ports.

21. (Currently Amended) An apparatus comprising:

means for counting statistics for a plurality of connections, wherein the statistics include a number of cells per connection of the plurality of connections and a number of cells having a loss priority bit;

means for determining if a count value for each of the connections is greater than or equal to a threshold; and

means for collecting the statistics for the connections of a ~~the~~ switch having ~~a~~ the count value greater than or equal to the threshold before connections having ~~a~~ the count value below the threshold.

22. (Cancelled)

23. (Currently Amended) The apparatus of claim 21, further comprising:

means for sending an interrupt signal from the means for counting statistics to a processor for each connection having the ~~a determined~~ count value greater than or equal to the threshold indicating that the statistics have a high priority.

24. (Currently Amended) The apparatus of claim 23, wherein the means for collecting statistics for connections with ~~corresponding~~ interrupt signals before other connections without ~~with no corresponding~~ interrupt signals.

25. (Original) The apparatus of claim 23, further comprising:

means for placing a logical connection identifier for each statistic having an associated count value above the threshold in a first-in-first-out (FIFO) buffer.

26. (Original) The apparatus of claim 25,

means for reading statistics in a memory based on the logical connection identifiers stored in the FIFO buffer.

27. (Currently Amended) A statistics collection module comprising:

a memory to store statistics for a connection, wherein the statistics include a number of cells per connection and a number of cells having a loss priority bit;

one or more module counters, each module counter to count the statistics stored in the memory;

a central processing unit (CPU) having internal CPU counters to count values from the one or more module counters, the CPU to determine if a count value for each of the module counters is greater than or equal to a threshold and to collect the statistics for the connections of ~~the~~ a switch stored in the memory derived from the module counters ~~having a~~ with the count value that is greater than or equal to the threshold before collecting statistics in the memory derived from the module counters having the count value below the threshold.

28. (Original) The statistics collection module of claim 27, wherein the internal CPU counters are wider than the one or more module counters.

29. (Original) The statistics collection module of claim 28, wherein the internal CPU counters are 64-bit counters and the one or more module counters are 32-bit counters.